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Rapid Design Exploration of Low Pass Highly Efficient Single Loop Single Bit Sigma Delta ($\Sigma\Delta$) Modulators

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A rapid design and verification of sigma delta modulators are presented at the system level with high accuracy and computational efficiency. Sigma delta analog to digital converters showcased an excellent choice for low bandwidth applications from near DC to high bandwidth standard 5G applications. The conceptualization of the graphical user interface (GUI) in the efficient selection of integrator weights has been proposed, which solves various tradeoffs between various abstraction levels. The sigma delta modulator of the 5th order is designed and simulated using the proposed design methodology of calculating integrator weights for targeted specifications. The efficiency of design exploration and optimum selection of integrator coefficients has been investigated on single loop architectures. Power and performance of the selected modulator has been verified in the time domain behavioral simulation. The discrete time circuit technique has been adopted for design of distributed feedback, feed forward architectures and comparison of performance metrics done between selected architectures. A huge design space is computed for the best design parameters that offers ultra-low power and high performance. The proposed virtual instruments supported the methodology for designing delta sigma modulators at the system level achieving SNDR of 122 dB over a bandwidth of 5 kHz at a clock frequency of 1 MHz.

Keywords: sigma delta modulator, single loop, time domain, virtual instruments, biomedical applications.

1. Introduction

Analog to digital converters (ADC) are integral part of complex integrated circuits acting as interface between analog and digital world, while digital to analog converters (DAC) translate digital codes into analog voltages or currents [1].

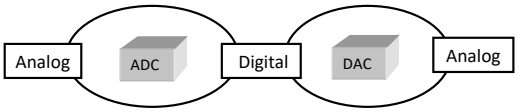

Fig. 1. Analog/Digital interface.

Ultra-low power design techniques in CMOS analog/digital interfaces facilitate efficient implementation of battery power complex circuits in modern health care applications. In recent years, invention of new technologies and advancements in electronic industry has brought rapid changes in human lifestyle, entertainment and especially healthcare services. Nowadays cardiovascular diseases are the major cause of death in the worldwide healthcare scenario. Advancements in wearable electronic sensor technologies enable the continuous observation of cardiac conditions of affected patients using all-day mobile health monitoring systems [2]. The analog front end along with high resolution and the energy efficient analog to digital (A/D) interface, shown in Fig. 1, is integrated into monitoring systems. The successive approximation register (SAR) ADCs consumes power of the nanowatt range limiting by anti-aliasing filter requirements. Sigma-delta ADC provides most efficient solutions for digitizing diverse types of signals in different application scenarios that include common bio-signals like electrocardiograms (ECG) shown in Fig. 2. The accuracy of the sigma-delta ADC depends on oversampling and quantization noise shaping which are the two major signal processing mechanisms in the A/D conversion. The sigma delta modulator ($\Sigma\Delta$M), performing sampling and quantization, is the dominant and power hungry block that influences the performance of sigma delta ADC. The analog signals detected by the sensor from the human body are extremely weak with low frequencies ranging from 0.05 (almost DC) to 2000 Hz. The useful band width of ECG is maximum of 1 kHz depending on application with the resolution of 12 bits. The high resolution ECG is required for late potential detection that prevents death from acute myocardial infarction.

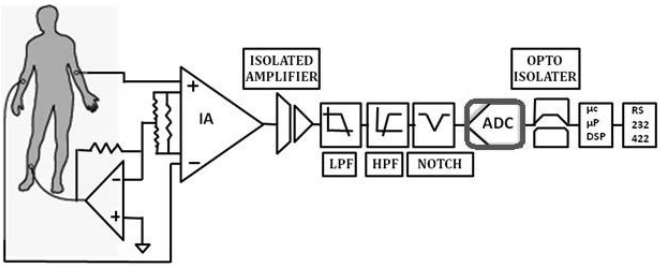

Fig. 2. ECG signal processing system.

The evolution of CMOS technology and advancements in sigma delta architectures lead the performance requirements of analog to digital conversion to

a peak. However, in practical situations, a real bottleneck in the design of sigma delta modulators exists at the system level rather than the circuit or device level, where the selection of modulator architecture, loop-filter topology, coefficients, and so on, can lead to a more efficient and robust design, while relaxing the design margins in the most critical metrics at an electrical level.

Application scenarios targeting high performance requirements (>20 bits resolution) obviously increase the complexity of the modulator system and dependency of performance on circuit errors. Estimation of design parameters are done at the initial stage of design with consideration of ideal equations but in practice, the circuit degrades the performance of a modulator. Various CAD tools are reported for design and simulation of sigma delta modulators at different levels of abstraction. Still there is a need of a rapid and simplified methodology for effective computation of design parameters and accurate estimation power and performance parameters, regardless of the modulator topology. The higher orders of SDMs (3rd, 4th, 5th and 6th) are implemented using FPAA (Field Programmable Analog Array) in Anadigm. The SDM architectures are designed and simulated in a time domain that supports reconfiguration of circuit architecture analogues to FPGA (Field Programmable Gate Array) in the design of digital systems. As the sigma delta modulator benefited with 10% of analogue and 90% of digital hardware the reconfigurable structures are well suited for prototyping of high performance mixed signal circuits. The AN221E04 device used for prototyping of a single loop and MASH SDMs using the SC circuit technique [3]. The proposed method suffers from accurate performance metrics evaluation of implemented SDM architectures in terms of resolution and power consumption even though it supports quick prototyping and testing of a circuit.

The majority of the $\Sigma\Delta$Ms reported by researchers implemented discrete time (DT) circuit techniques which covers the widest regions of resolution-versus-bandwidth plane. Power is a major entity along with performance when processing biomedical signals in wearable electronics. As the application demands the high resolution around 20 bits there is a tradeoff between power and performance. The modulator architecture selected in this work prevents multi stage DACs comparing to cascade architectures, anda quantization noise made dominant the compared circuit, thermal and other noises and by noise shaping the performance is improved. The following Eqs. (1) and (2) represent constraints of a circuit, nonlinearity, settling and quantization noise relation, respectively:

$$P_{cn} + P_{nl} + P_{st} \ll P_{qn}, \tag{1}$$

$$P_{qn} \cong \frac{1}{12}\left[\frac{2V_{\text{ref}}}{(2^b - 1)}\right]^2 \frac{\pi^{2L}}{(2L+1)\,M^{(2L+1)}}. \tag{2}$$

The authors in [4–7] presented DT ΣΔM for medical implant devices realized using active, active and passive loop filter variants with ultra-low power capabilities. The ΣΔMs investigated in that work. The continuous time (CT) SDMs are investigated in [7] and [8] using purely passive loop filters, active and passive combinations in [5] that occupied an extremely small area. The peak signal to the noise plus distortion (SNDR) achieved in [6] was 52 dB in the 250 Hz bandwidth dissipating the 540 nW power which is not suggestible for wearable devices. The third order ΣΔMin [8] using a passive loop filter achieved satisfactory SNDR of 69.1 in the 2 MHz bandwidth using only passive components as loop filters, the 1-bit quantizer. The second order ΣΔM was reported in three different variants for the 500 Hz signal bandwidth: a) both the loop filters are active stages, b) the first stage is active and a succeeding stage passive, c) both the loop filters as passive achieve the signal to noise plus distortion ratio (SNDR) of 76 dB, 70 dB and 67 dB, respectively in [4]. Increasing the noise shaping order in ΣΔM enhance the dynamic range (DR) in a good number of bits which is limited in passive loop filter implementations because of a signal attenuation. An alternative method to improve the DR is increasing the oversampling ratio (OSR) which leads to a large power consumption. Higher order modulators suffer from a stability problem using either active or passive loop filters in single loop architectures which can be prevented in the multi stage noise shaping (MASH) architectures. Matsukava *et al.* [11], proposed passive loop filter stages with a single operational amplifier (op amp) active resonator that reduce the power to great extent, but the performance of the proposed fifth order sigma delta modulator achieved 62.5 dB SNDR over the band width of 10 MHz. As the modulator using multi bit quantizer is applied the complexity also increases with DAC nonlinearity [9]. The resolution is the major drawback in existing works even though the power is optimized to nano-watts in the desired bandwidth, using variety of circuit techniques CT and DT, active and passive loop filter implementation [10, 11].

The objective of this work is to investigate a high resolution ΣΔM ADC interface for the ECG application without compromising the ultra-low power requirements in the 1 kHz bandwidth. An ideal case is the 3rd order sigma delta modulator using 1-bit quantizer capable of achieving approximately the 19-bit resolution with OSR of 100. But the actual scenario exhibits a degraded performance due to the various circuit level non-idealities and nonlinearities addressed in Sec. 2. The cascaded 3rd order switched capacitor sigma delta modulator achieved good DR of 110 dB over the bandwidth of 10 kHz using the chopper stabilization technique [12]. Multi stage noise shaping (MASH) architectures solves the stability issue with cascaded the first and second order stages. Ideally there is no degradation in performance of multi stage noise shaping architectures compared to a single loop architecture, but in reality circuit non idealities will af-

fect the noise shaping behavior in the higher order modulators. A Labview based virtual instruments are adopted in the system level design phase for the rapid estimation of optimum selection of integrator scaling for targeted performance.

The organization of this paper is as follows: the modulator topology selection for target specifications and the system level design consideration are discussed in Sec. 3. Section 4 presents behavioral modeling, analysis and ΣΔM for the investigated coefficients in time domain behavioral simulation. Section 5 represents circuit level implementation possibility, simulation results and performance comparison.

2. Non ideal and nonlinear effects design issues

The performance of sigma delta modulators may degrade due to a good number of circuit nonidealities and nonlinearities in analogue modulator blocks. Nonlinear effects of circuit elements have much more impact on the multi stage noise shaping architectures than single loop architectures preferred in this work. Still there is a need to consider the amplifier finite gain and the slew rate which generate the distortion and are the cause of an increase in the noise floor. These effects are different from continuous to discrete time implementation techniques. The most common non-ideal effects are associated with amplifiers, switches, capacitors, clock, multi-bit ADCs, and DACs.

For switched capacitor circuit implementations the ideal integrator transfer function (ITF) is:

$$\mathrm{ITF}(z) = \frac{z^{-1}}{(1 - z^{-1})}. \tag{3}$$

The practical integrator circuit deviates from Eq. (1) and non-ideal effects impose direct impact on NTF due to pole shifting from DC in an ITF. The transfer function of a practical integrator with the finite DC gain is represented as:

$$\mathrm{ITF}_{A_v}(z) = \frac{1}{1 + \left(1 + \frac{C_P}{C_I} + \sum_{i=1}^{N_i} \frac{C_{Si}}{C_I}\right) \frac{1}{A_v}} \frac{z^{-1}}{1 - z^{-1} \left[\frac{1 + \left(1 + \frac{C_P}{C_I}\right) \frac{1}{A_v}}{1 + \left(1 + \frac{C_P}{C_I} + \sum_{i=1}^{N_i} \frac{C_{Si}}{C_I}\right) \frac{1}{A_v}}\right]}. \tag{4}$$

The modulator output in z domain becomes very complex to estimate the integrator scaling coefficients as a result of the finite DC gain A_v and the parasitic capacitance C_P. For $A_v = \infty$ the above Eq. (4) simplified to the ideal case expression in Eq. (3), that makes the design feasible for a linear analysis. The

simplification of modulator output in z domain to Eq. (5) for the pure L-order noise shaping becomes a tedious task:

$$Y(z) = z^{-L}X(z) + \left(1 - z^{-1}\right)^{L} E(z). \tag{5}$$

Even though the choice of modulator topology selected in this work is less sensitive to circuit level nonidealities, a capacitor mismatch and A_v, still there exist few errors like circuit noise, jitter whose influence is independent of the modulator topology. The effect of a circuit noise is severe especially in the case of discrete time modulators.

3. System level modeling and design of ΣΔ modulator

A huge number of simulations need to be performed to fulfill the desired specifications in a high level synthesis of ΣΔ modulators. Depending on targeted specifications and design the iteration count may reach thousands or even more. At the high level synthesis a transistor level is inefficient due to vast resource consumption and large CPU time requirements. The design of the selected single loop architecture is presented in the form of flow chart, shown in Fig. 3.

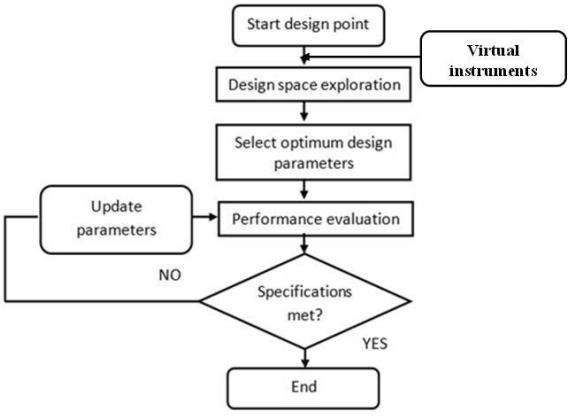

Fig. 3. Proposed design methodology flowchart.

The design parameters at this level are electrical specifications of modulator building blocks which are far away from the transistor length and widths. An alternative to the transistor level simulation at a high level synthesis trades the simulation time with accuracy using macro models popularly known as the multilevel simulation. Even the better simulation approach for evaluation of ΣΔ modulators reported [13–15] as behavioral simulation techniques with a high speed and acceptable accuracy in simulation results by giving best trade-off. EDA tools for the design of sigma delta modulators at different levels of abstractions are readily available from various industries and academic institutions. As

the design time and the cost are major constraints there is a need to identify a rapid and simplified approach for the design of sigma delta modulators with variety of architectures and implementation techniques. Figure 4 shows the single loop sigma delta modulator of the 5th order distributed feedback. The major problem of higher order modulators is well known stability due to magnification the quantizer input along with the modulator order. The stability of the sigma delta modulator depends on the quantizer input fed by a chain of integrators in single loop architectures. So, the integrator scaling should be computed carefully ensuring that the quantizer should not be overloaded. The performance of sigma delta modulator severely affected especially in higher order single loop architectures. Existing methods suffer from accuracy in integrator weights and the computation time which solved using highly efficient virtual instruments in GUI environment. If the gain coefficients of the integrators selected in such a way that the input to the quantizer is limited to a non-overloading value then the expected SNDR can be preserved at the other end the modulator stability also ensured.

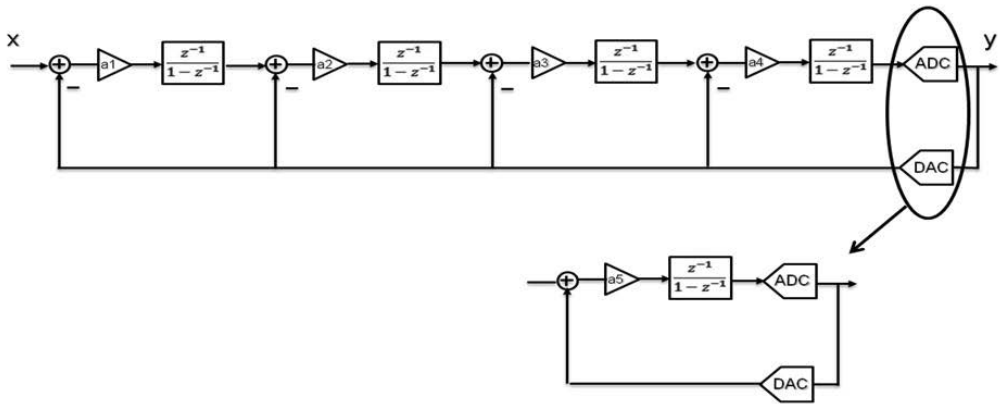

FIG. 4. Block diagram of fifth order single loop SDM.

The modulator output of the selected 5th order modulator yields:

$$Y(z) = \frac{k_q a_1 a_2 a_3 a_4 a_5 \frac{z^{-5}}{(1-z^{-1})^5} X(z) + E(z)}{A^*}, \tag{6}$$

where

$$A^* = 1 + k_q a_1 a_2 a_3 a_4 a_5 \frac{z^{-5}}{(1-z^{-1})^5} + k_q a_2 a_3 a_4 a_5 \frac{z^{-4}}{(1-z^{-1})^4} + k_q a_3 a_4 a_5 \frac{z^{-3}}{(1-z^{-1})^3} + k_q a_4 a_5 \frac{z^{-2}}{(1-z^{-1})^2} + k_q a_5 \frac{z^{-1}}{(1-z^{-1})},$$

a_1, a_2, a_3, a_4, and a_5 are integrator weights mentioned at the architecture level transformed into circuit level notation with the following relation:

$$a_1 = \frac{g_1' g_2}{g_2'}, \qquad a_2 = \frac{g_2' g_3}{g_3'}, \qquad a_3 = \frac{g_3' g_4}{g_4'}, \qquad a_4 = \frac{g_4' g_5}{g_5'}, \qquad a_5 = g_5',$$

where

$$g_1 = g_1^1 = \frac{C_{S11}}{C_{I1}},$$
$$g_2 = \frac{C_{S21} + C_{S22}}{C_{I2}}, \quad g_2^1 = \frac{C_{S22}}{C_{I2}}, \qquad g_3 = \frac{C_{S31} + C_{S32}}{C_{I3}}, \quad g_3^1 = \frac{C_{S32}}{C_{I3}},$$
$$g_4 = \frac{C_{S41} + C_{S42}}{C_{I4}}, \quad g_4^1 = \frac{C_{S42}}{C_{I4}}, \qquad g_5 = \frac{C_{S51} + C_{S52}}{C_{I5}}, \quad g_5^1 = \frac{C_{S52}}{c_{I5}}.$$

From Eqs. (7), (8) and (9) the expected dynamic range (DR) of the modulator by neglecting the finite amplifier gain and other non-linear and non-ideal effects calculated as 155 dB results 25.49 ENOB:

$$\mathrm{NTF}(z) = \left(1 - z^{-1}\right)^L. \tag{7}$$

For low frequencies, the approximated NTF

$$|\mathrm{NTF}(f)| = \left|1 - e^{\frac{-j2\pi f}{f_s}}\right|^L = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L \approx \left(\frac{2\pi f}{f_s}\right)^L. \tag{8}$$

The quantization noise power in band of interest with the noise shaping operation, where

$$\Delta = \frac{Y_{FS}}{(2^B - 1)}. \tag{9}$$

The practical DR and ENOB can be achieved closer to the ideal values by an optimum selection of design parameters specifically scaling coefficients. The following virtual instrument shown in Fig. 5 designed to generate scaling coefficients of the design space from which suitable values can be selected to transform Eq. (6) to (10):

$$Y(z) = z^{-5} X(z) + \left(1 - z^{-1}\right)^5 E(z). \tag{10}$$

The functional blocks used in the computation of integrator weights present the flat sequence structure for the computation of inter stage weights that satisfies the pure 5th order noise shaping behavior in Eq. (10). In addition to the above function While loop, random number generator, numeric, Boolean function and number to fractional string conversion functions are used.

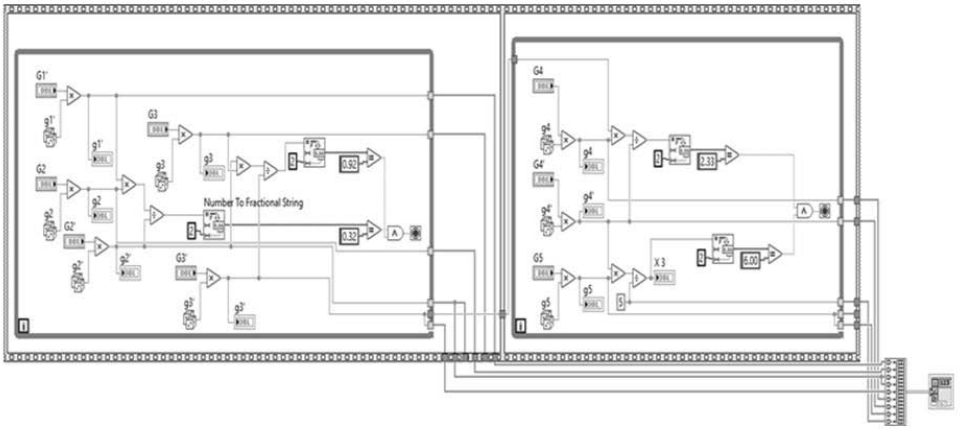

FIG. 5. Block diagram of integrator scaling computation virtual instrument.

Scaling coefficients computed here are useful for the circuit level implementation as modulator gain stages. This approach solves the major problem of the design time and cost in terms of number of iterations to select optimum design parameters which give stable performance. The front panel displays the scaling coefficients simplified as capacitor ratios that enable to minimize unit capacitors during the practical design phase. The stability of the modulator is verified for chosen scaling coefficients. Virtual instruments compute a vast design space in terms of scaling coefficients in less time which can be exported into a tabular format for the selection and construction of a transfer function model. Figure 6 shows the front panel of the virtual instrument that indicates few sets of coefficients and stability check results; g_1, g_1', g_2, g_2', g_3, g_3', g_4, g_4', g_5, g_5' are variable parameters that are computed in a front panel window.

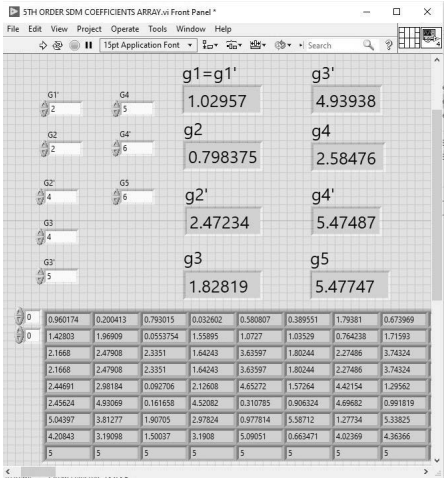

FIG. 6. Front panel of virtual instrument displaying integrator scaling.

Passive components as the integral part of the modulator are one of the choice for the modulator implementation which produce a low gain with which the output swing achievement is difficult to achieve. In order to maintain low power dissipation, the voltage scaling is the technique generally used which is supported by an integrator scaling selection from the above mentioned method [16, 17].

4. Simulation results

The performance of selected sigma delta modulator architecture is simulated using time domain behavioral models. At this stage the design parameters are the modulator building blocks parameters that include integrator scaling computed and other parameters that vary from a block to a block. The design parameters applied in a simulation process includes all possible non-ideal and non-linear effects of circuit elements ensuring the results obtained at the system level very close to circuit level implementations. The sigma delta modulator architecture is constructed using real integrators and comparator behavioral models in Simulink based sigma delta simulator. Critical errors of building blocks are applied while simulating the architecture to measure the performance with high accuracy and results are in close relation with lower level abstraction simulation results. Figure 7a shows the computed SNDR for the single loop of the 5th order modulator architecture by the FFT computation of a time domain output sequence. The signal spectrum and integrated noise power plotted for the obtained output sequence are shown in Figs. 7b and 7c.

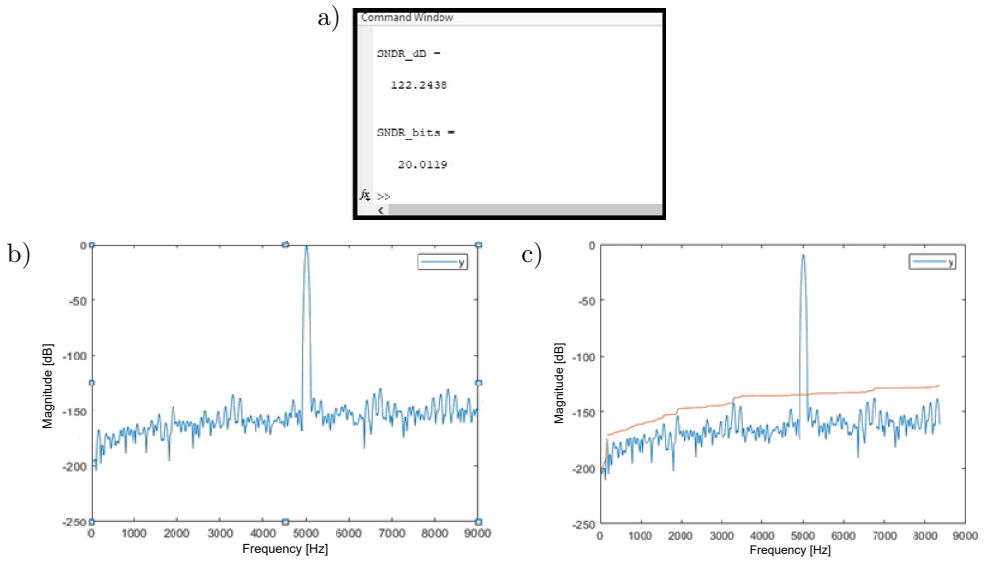

Fig. 7. a) SNDR computed, b) signal spectrum, c) integrated noise power.

The proposed modulator achieved 20 bit resolution with the oversampling ratio of 100 for the signal bandwidth of 5 kHz shown in Table 1. The works reported in [11] and [18] use the lower oversampling ratio when compared with the proposed modulator but the resolution achieved is not sufficient for the selected application. Roel and Kumar [3] achieved the high resolution and the signal bandwidth is not suitable for the required application. The high oversampling ratio modulator reported in [19] and [20] consumes a high power and is of the resolution also lower than compared to the proposed work.

Table 1. Performance comparison of proposed modulator.

Method	Over sampling ratio	Band width [Hz]	Signal to noise plus distortion ratio [dB]	Effective number of bits
Proposed work	100	5k	122	20
Lima *et al.*, 2016 [18]	64	1k	92.06	15
Matsukawa *et al.*, 2010 [11]	15	10M	62.5	11
Roel and Kumar, 2020 [3]	50	20k	71	12
Meimei *et al.*, 2016 [19]	256	250	140	22
Slim *et al.*, 2021 [20]	320	250	95	17.13

5. Conclusions

The higher order single loop sigma delta modulator of the fifth order is designed and verified and the possibility of an optimum design space of integrator coefficients is explored. The order of the modulator increases the design search space which leads to the increased design time and cost. The major constraint of the higher order loop stability is circumvented with the Labview assisted design parameter exploration. The proposed method simplifies the design process by a rapid estimation of design parameters saving the design time and cost. Even though Cascade architectures are the first choice for designers, the presented work enables selection of single loop modulators for high performance requirements, the stable modulator design. In the proposed method a lower number of simulations is to explore a huge design space and the optimum design parameters are selected. The modulator simulator in this approach reported the 20 bits resolution which is efficient compared to existing designs.

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